

Design Considerations of a Power Supply System for Fast Cycling Superconducting Accelerator Magnets of 2 Tesla B-Field Generated by a Conductor of 100 kA Current

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Abstract— Recently proposed fast cycling accelerators for proton drivers (SF-SPS, CERN and SF-MR, SF-BOOSTER, FNAL) neutrino sources require development of new magnet technology. In support of this magnet development a power supply system will need to be developed that can support the high current and high rate of power swing required by the fast cycling (1 sec rise and fall in the SF-MR, 5Hz in Booster). This paper will outline a design concept for a ± 2000 V and 100,000 A fast ramping power supply system. This power supply design is in support of a 6.44 km magnet system at 0.020 H and 330 m 5 Hz, 0.00534 H superconducting loads. The design description will include the layout and plan for extending the present FNAL Main Injector style ramping power supply to the higher currents needed for this operation. This will also include the design for a harmonic filter and power factor corrector that will be needed to control the large power swings caused by the fast cycle time. A conceptual design for the current regulation system and control will also be outlined. The power circuit design will include the bridge, filter and transformer plan based on existing designs.

Index Terms—Accelerator power supplies, Transmission-line conductors

I. INTRODUCTION

THE long-baseline neutrino oscillation search experiments require very high intensity neutrino beams. In support of this search two magnet systems using Fast-Cycling Superconducting Accelerator Components are being proposed [1]. This paper describes a power supply system for use on these magnets systems. The large machines, DSF-MR1-2 will provide beam to as many as 5 neutrino experiments at 480 GeV, while the booster will have a large aperture magnet and operate at 5 Hz and 8 GeV to increase the total beam power on target.

Manuscript received August 28 2007. Notice: This manuscript has been authored by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the U.S. Department of Energy. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this manuscript, or allow others to do so, for United States Government purposes.

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II. DEFINITION OF FAST CYCLING

The first goal of the DSF-MR machines is to increase the beam power on target using as much of the present infrastructure, Tevatron tunnel and cryogenics system as possible. This requires that we use all of the present booster cycles to maximize the amount of beam in the MI ring and then use two MI pulses to fill the each DSF-MR ring. To minimize the MI acceleration time the beam will only be accelerated to 40 GeV and then inject into one of the DSF-MR. This requires that we increase the RF system from the present 50 GeV per second in the Tevatron to 440 GeV per second (80 stations). The present Tevatron RF tunnel location only has room for 112 GeV (18 stations) worth of equipment so a second location for the rest of the stations will need to be constructed. This assumes that the two machines will be able to share the RF stations and will require at least two straight sections in the machines that are not used for extraction.

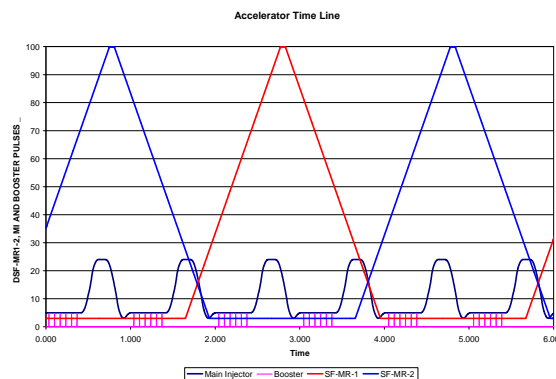


Fig.1. Ramp profile for two DSF-MR, two MI cycles are needed to fill the new machines, and 15 Booster cycles to fill the MI.

The cycle time for each machine is set by the present Booster and MI fill time and will remain at 4 seconds. If the flattop time is increased to allow for multi location extraction the cycle time will increase by this time. The MI ramp time will be reduced to 0.25 second because we only propose to accelerate to the 40 GeV level but will have a 1 one second cycle time controlled by the Booster fill time.

III. POWER SUPPLY LAYOUT

A. Power Supply Parallel Configuration

The MI power supply design will work for these magnet systems; we would need 10 in parallel with two in series, 20 in total instead of 12. However a new design for the power supplies could be constructed using the same topology, 12.5kA paralleled 360Hz full wave bridges. The 360 Hz Bridges will be supplied from one Delta-Delta and a Delta-Wye transformer then summed through the bridges and chokes to create a 720 Hz output. The DSF-MR machines will need ± 2000 volt while the 5 Hz booster will need a ± 315 volt version. The bridges are then summed through the filter bus work and impedance to assist in current sharing. A pair of transformers and bridges makes up a 25 kA power supply that is then parallel with three other supplies to create the 100kA supply needed. We presently use a paralleling scheme constructed of 6-5,000 A power supplies paralleled through filter chokes and bus work in a slow ramping application. In this application all the firing pulses for all six supplies are controlled from one regulator source. The regulation section, V. will outline the plan for this faster ramping power supply. The transformers will supply current through a bus duct system similar to the MI dipole power supplies [2]. Under a fault in the SCR bridge current will be source from the transformers limited by the bus duct impedance and back feed from the other parallel power supplies. The back feed current from the other power supplies in parallel will be limited by the choke impedance and bus work resistance. The choke design will need to have a leakage inductance of 70 μ H and a DC resistance of 220 $\mu\Omega$ with a bus work resistance of 196 $\mu\Omega$. With these impedances simulations show that the fault current will still be 250 kA at 40 m seconds when the vacuum circuit breaker, VCB opens. With some additional control to the bypass SCRs we will be able to reduce the risk of high current being back feed into the fault by relying on the 4 m seconds of the bypass to disconnect the other supplies from the fault.

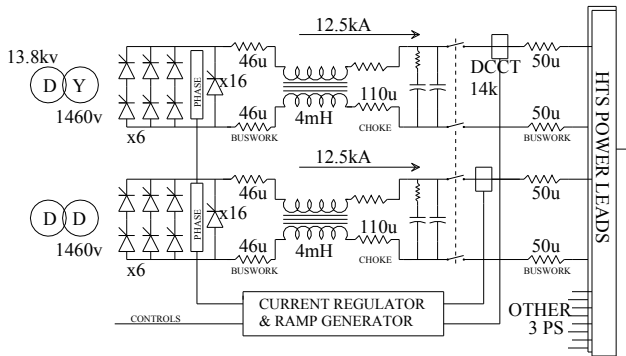


Fig.2 Parallel 12.5k A power supplies used to construct a 25k A section of the total power supply.

As with the MI dipole power supply these supplies will be constructed using 2.5 x 10 cm bus work including the windings in the choke. This bus has a DC resistance of 7 $\mu\Omega$ /m at 40 Deg C with a simple water cooling channel in the center. The bus duct system will also need to have improved bracing from the MI supply design to with stand the high forces from an SCR fault.

The disconnect switches shown in Fig. 2 are there to allow for the removal of one 25 kA power supply and filter sections for repair and allow the accelerator to operate at a lower energy. Due to the high current of this supply the power leads will need to be as close to the supply output as possible to reduce the need for 100 kA bus work. So the output of all the filter chokes will be connected at the warm end of the power leads.

The SCR Bridge will be constructed using the same design criteria as the MI but this supply will require an SCR that is higher voltage and current. To maintain the 80⁰ junction temperature used in the MI we will need to move to 100 mm devices. There are three sources for a 4400 volt and 100 mm device that will allow us to meet this design requirement. We will continue to use fiber optic gate trigger but will need an improved isolation transformer design for the firing circuit power due to the higher operating voltage.

B. Harmonic Filter Layout

The line side of this power supply will need to be constructed using two sources and four VCBs. This will allow us to maintain a 500 MVA fault system at the 13.8 kVA level and use VCBs of the same size we presently have in the Kuatz Road Substation, KRS for the main bus. When constructing a pulsed duty power system we specify our transformer to have a rating equal to the RMS plus $\frac{1}{2}$ the difference between the peak and RMS braced for pulse duty. This calculates to the 16 MVA shown in Fig. 3 for the rectify transformers.

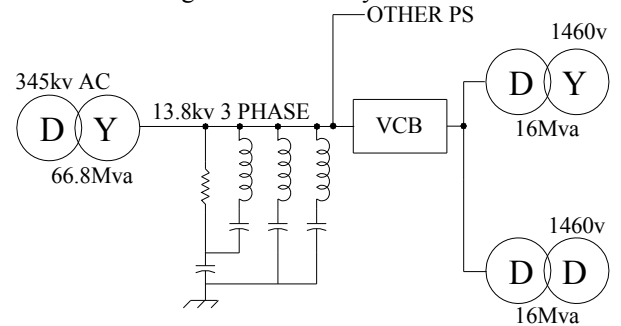


Fig.3 line input and harmonic filter layout.

The same design rules apply to the main power transformers. However the main ramping transformers will operate at 50% duty factor rather than 25% as seen by the rectify duty transformers. This means that we would need a 148 MVA power source. We have a pulse duty 66.8 MVA transformer on hand that can be relocated to power half of this power supply. A second transformer and substation will need to be added to this system. This is above our design criteria but within the operating rang of this particular transformer design.

With 200 MVA of power swing in and out of this supply we will need a higher power harmonic filter than the one used in the MI. The present filter has 10 MVA of damping power and will need to increase to 15 MVA. Using the 66.8 MVA transformers will require a new design for the filters due the leakage impedance change and higher harmonic power level.

IV. MAGNET SYSTEM PROTECTION

This is a fast cycling super conducting machine so the quench protection for the magnets can be much simpler than the TeV system. The magnet system total inductance is very low yet the stored energy is 100 MJ but can be removed quickly using the power supply. These accelerators only have one power supply that under normal ramping remove the energy stored from the magnets in one second. This may not be fast enough to remove the ring energy with out damage to the magnets during a quench without the use of bypass switches. We will finish the evaluation of magnet protection during the magnet design process. In the event that there is a quench and a power supply failure at the same time a Super Conducting Dump Switch system will be need. The decay time for the rings will be 330 second if the power supply just goes into bypass assuming a $140 \mu\Omega$ ring resistance and a - 6 volt drop on the power supply bypass SCRs.

A. Quench Detection System

The Quench Protection System, QPM will be reused from the TeV with slight modifications due to the low inductance per magnet. Each QPM will need to monitor 16 magnets per cell instead of the normal 4 to have a good signal to noise ration. This will allow the splitting of the QPM system into four parts with two used for the DSF-MR, part of the remaining two systems will be used for the Booster.

B. Superconducting Dump Switch

A super conducting dump switch design was developed for the VLHC [6] and would need to be constructed for these magnet systems. The dump switches will not be used under normal operation but only as a back up to a quench and power supply failure. This due to the amount of time it will take to cool back down from a full current dump. The plan is for a minimum of four switches to be installed in each ring which are backed up by each other. The resistance of the switch is chosen to create a voltage distribution to ground $\frac{1}{2}$ the normal power supply voltage, this allows for one or two switches not to open and still manage the magnet voltage while providing redundancy.

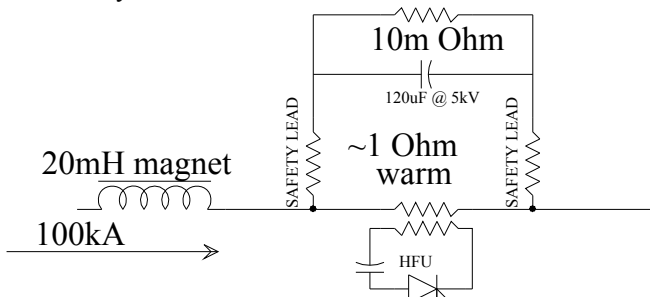


Fig.4 Superconducting Dump Switch used as a backup to the main power supply ramping down, one of four. A TeV style Heater Firing Unit HFU will be reused to trigger the dumps.

V. CURRENT REGULATION

The current regulator will be modeled after the Fermilab Main Injector ramping computer, MECAR [4]. In the Main Injector, MI implementation of the learning computer a voltage program is sent to the voltage regulator of each power

supply that provide closed voltage loop regulation. In the MI, power supplies are dispersed around a two mile ring and connected in series. In the plan for the DSF-MR system the four power supplies will be in a single location, one set for each ring. This will allow for local control of the power supply output. The regulation computers will have direct control of the firing pulse to the SCR's in the output bridge. With the four power supplies in parallel, small changes in the voltage regulation will make large changes in the output current. Using a closed loop voltage regulation scheme would require a very high precision voltage feedback scheme to avoid over currents in any one of the bridges. Operating the bridges in open loop/phase mode from the ramping computers will improve the current balance between supplies. Open loop regulation will require that the ramping computer compensate for line voltage sage during the ramp to ensure a reasonable current balance and tack the current reference.

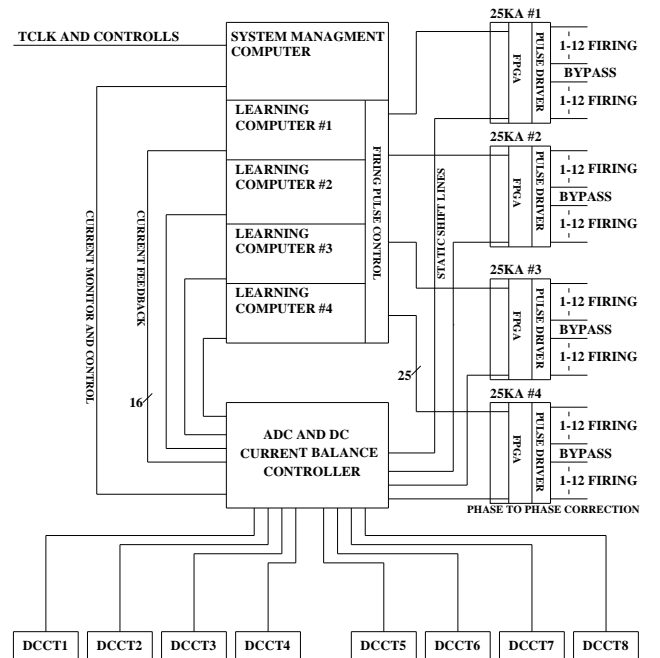


Fig.5. MECAR (Main Ring Excitation Controller and Regulator) based current regulation system.

The gate firing circuits will need to have a DC fine tunable correction system that will correct for the small time differences in the SCR firing while the power supply is at low voltage. This is the point that the voltage gain per unit of time is the largest and any dispersion in firing angle can cause a current imbalance. In addition this will also reduce sub-harmonic ripple caused by voltage difference per phase.

Operation of this current regulator will rely on the impedance in the system to manage the bulk current balance in the bridges. The current regulator will provide the necessary phase angle adjustment to provide the voltage needed for the current during the ramp cycle including line sage correction. The balance controller will generate a total current from the summation of the eight DCCTs in the circuit feedback through the ADC controller. The current balance controller will also generate a current error from a programmed current reference and each DCCT measurement. These error signals will then be minimized using a learning algorithm in the current

regulator for each bridge by adjusting the phase angle for each pulse in the bridge as needed.

VI. BOOSTER MAGNET SYSTEM

The decay time for the stored energy in this machine is controlled by the resistance in the load. We have shown the magnet system Fig. 6 with quench bypass switches to allow time for the magnet system to de-excite the magnet under a quench condition. The power supply on this system can not remove the energy fast enough to protect the magnets. This system will also need at least two of the super conducting dump switch used in the DSF-MR rings and bypass switches.

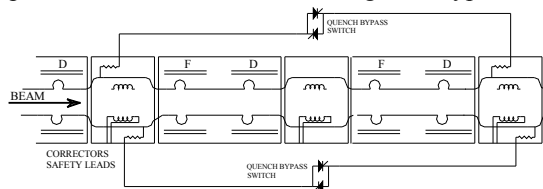


Fig.6 Booster magnet system layout showing the quench bypass switches.

The bypassing cable will be installed internal to the magnet in the outer vacuum chamber inside of a cooling tube. These cables and SCR's will only be cooled during and after a quench using a control valve in the helium system. The switches for this system will be of a new design but will be able to reuse the Tev QPMs and Quench Bypass Switch controllers.

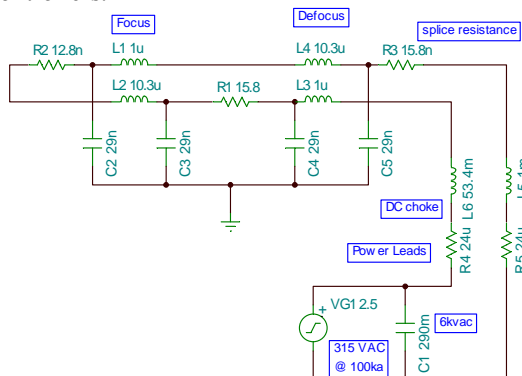


Fig.7 Booster power system layout simulation model.

VII. BOOSTER MAGNET POWER SYSTEM

The booster power supply will need the added elements for the resonance circuits, a 0.29 F cap at 10 kV and a 0.0534 H inductor. This model has the ring split into in half with two magnet models representing the total magnet inductance. The power supply for this ring is a voltage regulated source at 315 V rather than a current regulated but will still need the current regulation for the balance circuit.

A. Capacitor Bank Issues

This system needs a very large high voltage cap bank with an operational stored energy of 10 MJ and will also need to handle the very high current. The Q of this circuit is very high, 3200 and the bandwidth is narrow, 0.0015 Hz. To get the tune correct the cap bank will need to be constructed using many elements that will allow for fine adjustment to the total

value. This should not be a problem due the high current requiring many current paths and many individual capacitor elements. The fault current management will require a substantial effort to protect the individual caps from the total energy in both the bank and the magnets.

B. Resonant Choke Issues

The present simulations of the magnet string uses a choke that is 10 times the magnet inductance, this is a large choke. With a reasonable effort a better choice for the inductance and cap bank value should be achievable and manageable. It will need to be a superconducting choke due to the high current and should be constructed using the HTS wire similar to the magnet load. This will require a different coil design constructed of many turns in the core and still manage the coil losses at 5Hz.

VIII. CONCLUSION

Providing power to these magnet systems requires a very large power supply. Development of this supply will require an R&D program consisting of the construction of at least one of the 25 kA sections which include the choke and bus work layout. The current regulator will also need to be constructed as part of this development but can be completed using a small model of the overall system. A program for the construction of the super conducting dump switch will also need to be completed as part of the R&D program. The design of the Booster choke will need a reasonable amount of R&D effort using the HTS wire wound in a coil and operated at 5 Hz.

ACKNOWLEDGMENT

Steven Hays thanks Gijsbert de Rijk and Lucio Rossi of CERN for their support of this development.

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